UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,939	07/31/2003	Gerard Chauvel	TI-35710 (1962-05423)	9644

23494 7590 12/23/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,939	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending.

2. The office acknowledges the following papers:

Foreign priority papers filed on 3/15/2004,

Oath filed on 12/8/2003.

Priority

3. This application claims priority to provisional application 60/400,391. The effective filing date for those claims which have proper support in the provisional application is 7/31/2002.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation from claim 8 "including data flags that indicate coherence" must be shown or the feature(s) canceled from the claim(s). Figures 6 and 7 show a "syschronization unit," and should be changed to "synchronization unit." No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Specification

5. The disclosure is objected to because of the following informalities:

6. The section titled cross-reference to related applications cites cases related, but leaves out the serial numbers. The serial numbers of the applications should be added, or the patent numbers should be added if applicable.

7. The specification must describe all claimed elements. Therefore, the limitation from claim 8 "including data flags that indicate coherence" must be described in the specification.

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

9. Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 3, 12, and 19 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "the local variables associated with the called method use data memory space previously used by local variables associated with completed method without generated a miss" is unclear. It's unclear if this limitation is to be interpreted as a method call will never result in generating a miss or if some method calls don't generate a miss. The specification doesn't support method calls never generating a miss. If enough nested methods are called, then the

D-RAMset will fill up from storing all of the local variables from the method calls. This will result in some of the local variables being saved away in main memory, which will later generate a miss on local variables (Specifications paragraph 47). For claim interpretation, the limitation will be interpreted as some method calls don't generate a miss.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-3, 5-12, and 14-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984).

14. As per claim 1:

Feierbach disclosed a system, comprising:

A first processor (Feierbach: Figure 2 element 204, column 6 lines 53-67 continued to column 7 lines 1-7);

A second processor coupled to the first processor, the second processor having a core and comprising stack storage residing in the core (Feierbach: Figure 2 elements 202 and 210, column 6 lines 53-67 continued to column 7 lines 1-7);

Memory coupled to, and shared by, the first and second processors (Feierbach:

Figure 2 element 212, column 6 lines 53-65)(The data cache is shared by the two processors.); and

A synchronization unit coupled to the first and second processors, said synchronization unit synchronizes the execution of the first and second processors (Feierbach: Figure 4 element 402, column 10 lines 25-55)(The copy unit monitors data accesses and ensures that data is properly exchanged between processors and other memory units. Thus having the same functionality.);

Wherein the second processor executes stack-based instructions (Feierbach: Figure 2 element 202, column 6 lines 53-65) while the first processor executes one or more tasks (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1, column 3 lines 20-67) wherein the first processor manages the memory via an operating system that executes only on the first processor (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1 elements 44a-b, column 3 lines 20-67)(Yung manages memory through the memory management units.) and the second processor executes a virtual machine that controls the execution of a program on the second processor (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 1 element 100, column 5 lines 35-54)(The stack processor runs a virtual machine that controls the execution of instructions.).

Feierbach failed to teach the first processor executes a virtual machine that controls the execution of a program on the second processor.

However, Seal disclosed the first processor executes a virtual machine that

controls the execution of a program on the second processor (Seal: Figure 18 element 326, column 16 lines 38-48; Figure 20, column 17 lines 38-67)(The processor includes a virtual machine to execute Java bytecodes. Some of the instructions can't be run on the processor, and are executed by software. Thus having the same functionality.).

An advantage of having the first processor process Java bytecodes through acceleration techniques is that the instructions will run faster on the hardware as opposed to the software executing the instructions (Seal: Column 1 lines 19-47). The instructions that are too complex to be executed on hardware are sent off to be executed on software (Seal: Column 1 lines 19-47). One of ordinary skill in the art would have been motivated to use a virtual machine to assist in accelerating Java bytecode instructions for the benefit of increased performance from the accelerated instructions being executed in hardware. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a virtual machine to help accelerate Java bytecodes for the advantage of increased performance.

15. As per claim 2:

Feierbach and Seal disclosed the system of claim 1 wherein the second processor comprises an internal data memory that holds a contiguous block of memory defined by an address stored in a register, and wherein local variables are stored in said data memory (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11).

16. As per claim 3:

Feierbach and Seal disclosed the system of claim 2 wherein the second

processor executes methods (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11) and wherein when a new method is called by the second processor, the local variables associated with the called method use data memory space previously used by local variables associated with completed methods without generating a miss (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11)(The stack won't generate a miss as long as the stack isn't filled up with storage from other nested methods.).

17. As per claim 5:

Feierbach and Seal disclosed the system of claim 1 wherein the stack-based instructions comprise Java bytecodes (Feierbach: Column 5 lines 4-29) and the first processor comprises a RISC processor (Seal: Figure 10 element 12, column 5 lines 60-67 continued to column 6 lines 1-9) so that the RISC processor executes one or more tasks while the second processor executes Java code.

18. As per claim 6:

Feierbach and Seal disclosed the system of claim 1 further including a main stack residing outside the second processor's core and coupled to the stack storage in the second processor's core (Feierbach: Figure 2 element 212, column 7 lines 8-18).

19. As per claim 7:

Feierbach and Seal disclosed the system of claim 6 wherein the stack storage in the second processor's core provides an operand to execute a stack-based instruction in the second processor (Feierbach: Figure 2 element 210, column 7 lines 50-65).

20. As per claim 8:

Feierbach and Seal disclosed the system of claim 6 further including data flags that indicate coherence between the main stack outside the second processor's core and data within the stack storage in the second processor's core (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4c element 151, column 19 lines 25-54)(The dribble management unit ensures coherency between the processor stack and the main stack.).

21. As per claim 9:

Feierbach and Seal disclosed the system of claim 8 wherein coherency is established by examining the data flags and updating the main stack with values from the stack storage (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4c element 151, column 19 lines 25-54)(The dribble management unit ensures coherency between the processor stack and the main stack.).

22. As per claim 10:

Claim 10 essentially recites the same limitations of claim 1. Therefore, claim 10 is rejected for the same reasons as claim 1.

23. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

24. As per claim 12:

Claim 12 essentially recites the same limitations of claim 3. Therefore, claim 12 is rejected for the same reasons as claim 3.

25. As per claim 14:

Claim 14 essentially recites the same limitations of claims 6-7. Therefore, claim 14 is rejected for the same reasons as claims 6-7.

26. As per claim 15:

Claim 15 essentially recites the same limitations of claims 6 and 8. Therefore, claim 5 is rejected for the same reasons as claims 6 and 8.

27. As per claim 16:

Claim 16 essentially recites the same limitations of claim 9. Therefore, claim 16 is rejected for the same reasons as claim 9.

28. As per claims 17-18:

Claim 17-18 essentially recites the same limitations of claim 1-2. Therefore, claim 17-18 is rejected for the same reasons as claim 1-2.

29. As per claim 19:

Claim 19 essentially recites the same limitations of claim 3. Therefore, claim 19 is rejected for the same reasons as claim 3.

30. Claims 4 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), further in view of Jain (U.S. 6,954,873)

31. As per claim 4:

Feierbach and Seal disclosed the system of claim 1.

Feierbach and Seal failed to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode.

However, Jain disclosed wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode (Jain: Figure 6a, column 3 lines 6-34).

The advantage of using a synchronization unit to check data accesses is to avoid accessing corrupt or old data (Jain: Column 1 lines 49-58). The use of a wait signal can tell another processor that a current piece of data is being used elsewhere. One of ordinary skill in the art would have been motivated to check memory accesses and use wait signals for the advantage of upholding data integrity. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement wait signals for processors accessing data for the advantage of preventing data corruption and upholding data integrity.

32. As per claim 13:

Claim 13 essentially recites the same limitations of claim 4. Therefore, claim 13 is rejected for the same reasons as claim 4.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sexton et al. (U.S. 6,775,763), taught a RISC and stack-based system of executing java bytecodes that execute complex bytecodes through emulation.

Evoy et al. (U.S. 5,953,741), taught a RISC and stack-based system where the RISC processor controls the stack-based processor and the RISC processor is able to execute native instructions as well as instructions native to the stack-based processor.

Koppala (U.S. 6,009,499), taught memory coherence for a stack-based processor.

Leung et al. (U.S. 6,009,509), taught a system that can change from a register-based processor to a stack-based processor for a temporary basis.

Grove (U.S. 6,205,578), taught virtual machines for register-based processors to execute Java bytecodes.

Poff et al. (U.S. 6,330,659), taught a Java accelerator to execute Java bytecodes.

Patel et al. (U.S. 6,826,749), taught a Java accelerator for a register-based machine that can execute Java bytecodes.

Raz et al. (U.S. 6,606,743), taught a Java accelerator for a register-based machine that can execute Java bytecodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183